IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer, the bulk growth layer including a silicon bulk growth layer and a silicon germanium bulk growth layer;

a first isolation formed in the bulk device region so as to separate the bulk device;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; ~~and~~

a second isolation formed in the SOI device region so as to separate the SOI device; and

a boundary layer located at ~~the~~ a boundary between the bulk device region and the SOI device region.

Claim 2 (Original): The semiconductor chip according to claim 1, wherein the bulk growth layer is a silicon bulk growth layer, and the boundary layer reaches the base substrate and is made of one of polysilicon or silicon-based compound semiconductors.

Claim 3 (Previously Presented): The semiconductor chip according to claim 1, wherein the first and second isolations are of substantially the same depth.

Claim 4 (Original): The semiconductor chip according to claim 3, wherein the first and second isolations have a depth reaching the buried insulator.

Claim 5 (Currently Amended): A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer;

a pn junction formed in the bulk device region and positioned above an interface between the base substrate and the bulk growth layer;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; ~~and~~

a first isolation formed in the bulk device region so as to separate the bulk device, and a second isolation formed in the SOI device region so as to separate the SOI device, the first and second isolations being substantially the same depth and having a depth reaching the buried insulator; and

a boundary layer located at a boundary between the bulk device region and the SOI device region.

Claim 6 (Currently Amended): The semiconductor chip according to claim 1, further comprising ~~a first isolation in the bulk device region, a second isolation in the SOI device region, and~~ a third isolation positioned at the boundary and functioning as the boundary layer, wherein the first, second, and third isolations are of substantially the same depth.

Claim 7 (Currently Amended): A semiconductor chip comprising:

a base substrate;

a bulk device having a bulk growth layer on a part of the base substrate, the bulk region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer,

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; and

a first isolation in the bulk device region, a second isolation in the SOI device region, and a third isolation positioned at ~~the~~ a boundary between the bulk device region and the SOI device region and functioning as a boundary layer located at [[a]] the boundary ~~between the bulk device region and the SOI device region~~, the first, second, and third isolations being deeper than the buried insulator.

Claim 8 (Previously Presented): The semiconductor chip according to claim 7, wherein the third isolation has a sidewall that is in contact with the buried insulator.

Claim 9 (Currently Amended): The semiconductor chip according to claim 7, wherein the bulk device region has ~~A semiconductor chip comprising:~~

~~a base substrate;~~

~~a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device fabrication surface in which a bulk device is positioned on the bulk growth layer;~~

a pn junction ~~formed in the bulk device region and~~ positioned below an interface between the base substrate and the bulk growth layer[[;]]

~~an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; and~~

~~a boundary layer located at a boundary between the bulk device region and the SOI device region~~.

Claim 10 (Currently Amended): The semiconductor chip according to claim 1, further comprising ~~a first isolation in the bulk device region, a second isolation in the SOI device region, and~~ a third isolation positioned at the boundary and functioning as the boundary layer, wherein the second isolation is shallower than the third isolation.

Claim 11 (Currently Amended): The semiconductor chip according to claim 1, further comprising the first isolation in the bulk device region, and the second isolation that is shallower than the first isolation, wherein the boundary layer is whichever of the first or the second isolation that is positioned closest to the boundary.

Claim 12 (Previously Presented): The semiconductor chip according to claim 11, wherein the second isolation functions as the boundary layer, and has a bottom face that is in contact with the buried insulator.

Claim 13 (Original): The semiconductor chip according to claim 1, further comprising a dummy pattern in the bulk device region near the boundary.

Claim 14 (Previously Presented): A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device including a DRAM cell having a trench capacitor, is positioned on the bulk growth layer;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level;

a boundary layer located at a boundary between the bulk device region and the SOI device region; and

a dummy pattern formed in the bulk device region near the boundary, the dummy pattern being a dummy capacitor.

Claim 15 (Original): The semiconductor chip according to claim 1, wherein the bulk device positioned in the bulk device region includes a DRAM cell having a trench capacitor, the trench capacitor comprising a first part extending at and below the interface between the base substrate and the bulk growth layer, and a second part extending above the interface, the width of the first part being greater than that of the second part.

Claim 16 (Withdrawn): A method for fabricating a semiconductor chip comprising:

preparing an SOI substrate consisting of a base substrate, a buried insulator on the base substrate, and a silicon layer on the insulator;

removing the silicon layer and a portion of the buried insulator in a predetermined area of the SOI substrate;

forming a sidewall protection film covering a side face of the silicon layer revealed by the removal;

exposing the base substrate in said predetermined area;

forming a bulk growth layer from the exposed surface of the base substrate until the top face of the bulk growth layer is in alignment with the top face of the silicon layer;

forming isolations having the same depth in the bulk growth layer and in the SOI substrate in a same process; and fabricating devices in the bulk growth layer and the silicon layer on the buried insulator.

Claim 17 (Withdrawn): The method according to claim 16, wherein the base substrate is exposed by wet etching.

Claim 18 (Withdrawn): The method according to claim 16, further comprising:

removing the sidewall protection film after the formation of the bulk growth layer,

wherein the fabrication of devices includes forming a gate and filling a recess resulting from the removal of the sidewall protection film with a semiconductor gate material.

Claim 19 (Withdrawn): The method according to claim 18, wherein the semiconductor gate material includes polysilicon and silicon-based compound semiconductors.

Claim 20 (Withdrawn): The method according to claim 16, wherein the formation of isolations includes providing isolation at the boundary between the bulk growth layer and the SOI substrate, while removing the sidewall protection film.

Claim 21 (Withdrawn): A method for fabricating a semiconductor chip comprising:

preparing an SOI substrate consisting of a base substrate, a buried insulator on the base substrate, and a silicon layer on the insulator;

removing the silicon layer at a first position of the SOI substrate to form a first isolation in the removed portion, a side face of the silicon layer being covered with the first isolation;

exposing a top face of the base substrate at a second position, while keeping the side face of the silicon layer covered with the first isolation;

forming a bulk growth layer from the exposed surface of the base substrate until the top fate of the bulk growth layer is in alignment with the top face of the silicon layer;

forming a second isolation in the bulk growth layer, the second isolation being deeper than the first isolation; and

fabricating devices in the bulk growth layer and the silicon layer on the buried insulator.

Claim 22 (Withdrawn): The method according to claim 21, wherein the formation of the first isolation includes providing an isolation at a position that is to be a boundary between the bulk growth layer and the SOI substrate.

Claim 23 (Withdrawn): The method according to claim 21, wherein the formation of the first isolation includes providing an isolation to the second position at which the base substrate is to be exposed.

Claim 24 (Withdrawn): The method according to claim 21, further comprising:

forming a first part of a trench capacitor in the exposed surface of the base substrate before the bulk growth layer is formed, the first part having a first width; and

forming a second part of the trench capacitor in the bulk growth layer, the second part being connected to the first part and having a second width narrower than that of the first part.

Claim 25 (Withdrawn): A method for fabricating a semiconductor chip comprising:

preparing an SOI substrate consisting of a base substrate, a buried insulator on the base substrate, and a silicon layer on the insulator;

removing the silicon layer and the buried oxide in a predetermined area of the SOI substrate to expose the base substrate;

forming a first part of a trench capacitor in the exposed base substrate;

forming a bulk growth layer on the exposed base substrate until the top face of the bulk growth layer is in alignment with the top face of the silicon layer on the buried insulator, and forming a second part of the trench capacitor connected to the first part and having a second width narrower than the first width.

Claim 26 (Withdrawn): The method according to claim 25, further comprising:

forming isolations in the bulk growth layer and in the SOI substrate in the same process.

Claim 27 (Withdrawn): A method for fabricating a semiconductor chip comprising:

preparing an SOI substrate consisting of a base substrate, a buried insulator on the base substrate, and a silicon layer on the insulator;

removing the silicon layer and the buried oxide in a predetermined area of the SOI substrate to expose the base substrate;

forming a bulk growth layer on the exposed base substrate until the top face of the bulk growth layer is in alignment with the top face of the silicon layer on the buried insulator;

forming a dummy pattern in the bulk growth layer near the boundary with the SOI substrate, the dummy pattern being deeper than the buried insulator; and

fabricating devices in the bulk growth layer and in the SOI substrate.

Claim 28 (Withdrawn): The method according to claim 27, wherein the formation of the dummy pattern includes forming a trench capacitor in the bulk growth layer in the same process as for forming the dummy pattern.

Claim 29 (Previously Presented): The semiconductor chip according to claim 1, wherein the bulk device positioned in the bulk device region includes a DRAM cell having a trench capacitor and a MOSFET, wherein the MOSFET is positioned between the DRAM cell and the boundary layer.

Claim 30 (Currently Amended): ~~The semiconductor chip according to claim 1, wherein~~ A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer, the bulk growth layer ~~is~~ being a silicon germanium bulk growth layer;

a first isolation formed in the bulk device region so as to separate the bulk device;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level;

a second isolation in the SOI device region so as to separate the SOI device; and

a boundary layer located at a boundary between the bulk device region and the SOI device region.

Claim 31 (Canceled).